



QUAD SURFACE MOUNT TVS ARRAY

Features

- Quad TVS in Common Anode Configuration
- Ultra-Small Surface Mount Package
- Ideal For Transient Suppression and ESD Protection
- Low Capacitance, <10pF @ V_R = 0V
- Lead Free By Design/RoHS Compliant (Note 1)
- "Green Device" (Note 2)
- Qualified to AEC-Q101 Standards for High Reliability

ESD Capability

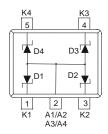
- IEC 61000-4-2 Contact Method ±8kV
- IEC 61000-4-2 Air Discharge Method ±15kV

Mechanical Data

- Case: SOT-953
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish: Matte Tin, Annealed Over Copper Leadframe.
 Solderable per MIL-STD-202, Method 208
- Weight: 0.002 grams (approximate)



Top View



Device Schematic

Ordering Information (Note 3)

Part Number	Case	Packaging
DUP412VP5-7	SOT-953	10,000/Tape & Reel

Notes:

- 1. No purposefully added lead.
- 2. Diodes Inc.'s "Green" policy can be found on our website at http://www.diodes.com/products/lead_free/index.php.
- 3. For packaging details, go to our website at http://www.diodes.com.

Marking Information



V1 = Product type marking code



Thermal Characteristics

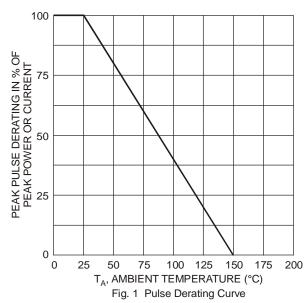
Characteristic	Symbol	Value	Unit
Peak Power Dissipation, 8x20μS Waveform (Note 5)	P _{pk}	18	W
Thermal Resistance, Junction-to-Ambient (Note 5)	$R_{ hetaJA}$	417	°C/W
Operating and Storage Temperature Range	T _{J,} T _{STG}	-55 to +150	°C

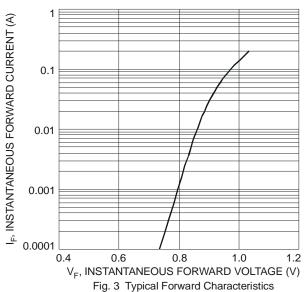
Electrical Characteristics @TA = 25°C unless otherwise specified

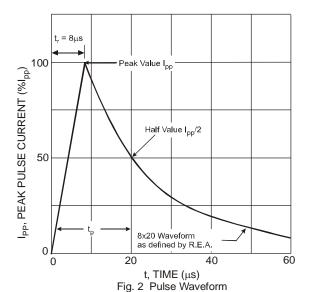
Туре	Marking	Breakdown Voltage (Note 6)		Leakage Current (Note 6)		Capacitance @0V Bias(pF) (Note 7)		Capacitance @3V Bias(pF) (Note 7)		
Number	Code	VE	_{BR} @ I _T = 5m	Α	I _{RM} @	V _{RM}	С	Τ	O	Ť
		Min (V)	Nom (V)	Max (V)	Max(μA)	(V)	Тур	Max	Тур	Max
DUP412VP5	V1	11.4	12	12.7	0.5	9.0	6.5	10	3.5	5

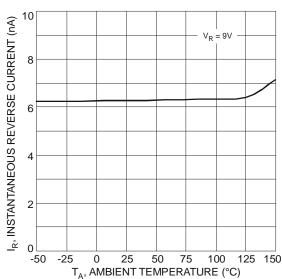
Notes:

- 4. Non-repetitive current pulse per Figure 2 and derate above T_A = 25°C per Figure 1.
- 5. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch; pad layout as shown on Diodes Inc. Suggested Pad Layout Document AP02001, which can be found on our website at http://www.diodes.com.
- 6. Short duration pulse test used to minimize self-heating effect.
- 7. Per element, f = 1MHz, $T_A = 25^{\circ}C$

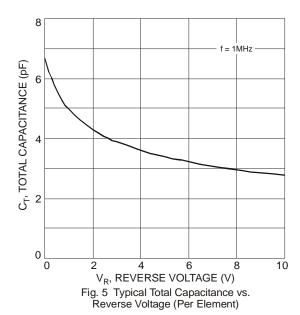




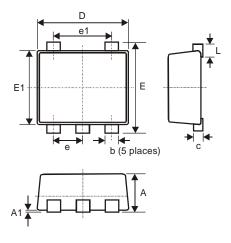






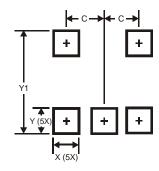


Package Outline Dimensions



SOT-953					
Dim	Min	Max	Тур		
A	0.40	0.50	0.45		
A1	0	0.05	-		
b	0.10	0.20	0.15		
C	0.12	0.18	0.15		
D	0.95	1.05	1.00		
Е	0.95	1.05	1.00		
E1	0.75	0.85	0.80		
е	-	-	0.35		
e1	_	-	0.70		
L	0.05	0.15	0.10		
All Dimensions in mm					

Suggested Pad Layout



Dimensions	Value (in mm)
С	0.350
Х	0.200
Y	0.200
Y1	1.100



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